

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): Method for generating an internal sequence of analog values that are synchronous to an external sequence coded in a received signal, the analog values having a specific period, which corresponds to and is synchronous with an the external sequence coded in a received signal and is synchronous with it, and the external sequence comprising repetitions of a fundamental sequence (s_1, \dots, s_N) of length N, which substantially corresponds to a sequence of binary values which can be produced by logical combination of a first generating binary sequence (p_1, \dots, p_N) of length N with a non-constant second generating binary sequence (q_1, \dots, q_N) of length N, ~~and the first generating binary sequence (p_1, \dots, p_N) being capable of being generated by a binary feedback shift register of length n, in which a next value (p_i) of the first generating binary sequence is produced in each case by binary logical combination of the an oldest value (p_{i-n}) of the binary feedback shift register with at least one of the values $(p_{i-n+1}, \dots, p_{i-1})$ subsequent value of the binary feedback shift register following the oldest value, following it, according to a fixed feedback pattern, and in which no segment of the length n occurs more often than once in the fundamental sequence, so that the position of such a segment is uniquely determined within with respect to the fundamental sequence (s_1, \dots, s_N) , characterized in that in each case the method comprising:~~

producing an intermediate value by a logical combination of an actual value of the external sequence with an actual value of a second generating sequence;

producing an input value to an analog feedback shift register by superposition of the intermediate value with an analog feedback value derived according to a feedback function from analog values in the analog feedback shift register, the analog feedback shift register having a length n and including a feedback pattern corresponding to a feedback pattern of the binary feedback shift register;

~~feeding a new the~~ input value (a_i) ~~is fed to the an~~ input of ~~an the~~ analog feedback shift register of length n ~~with a feedback pattern corresponding to that of said binary feedback shift register, which input value is produced by superposition of an analog feedback value derived from the values (a_{i-n}, \dots, a_{i-1}) in the analog feedback shift register according to a feedback function with an intermediate value which was produced by a logical combination of the actual value of the external sequence with an actual value (q_i) of the second generating sequence (q_1, \dots, q_N), the ; and~~

~~a position (i) of which of an~~ actual value ~~therein of the second generating sequence~~ follows ~~the corresponding to a position of a segment in with respect to~~ the first generating sequence (p_1, \dots, p_N), ~~which, the segment consists of including~~ a determinative set of n binary values ~~which were derived from the analog values (a_{i-n}, \dots, a_{i-1}) in the analog feedback shift register.~~

Claim 2 (Currently Amended): Method according to Claim 1, ~~characterized in that~~ wherein the first generating sequence (p_1, \dots, p_N) ~~is~~ includes an m -sequence of length $N = 2^n - 1$, so that each set of n binary values, except for one, occurs exactly once as a segment of length n therein.

Claim 3 (Currently Amended): Method according to Claim 2, ~~characterized in that~~ wherein the fundamental sequence is a Gold sequence.

Claim 4 (Currently Amended): Method according to ~~any of Claims~~ Claim 1 ~~to 3,~~ ~~characterized in that~~ further comprising:

reading from a table the actual value (q_i) of the second generating binary sequence (q_1, \dots, q_N) ~~is in each case read out from a table with~~ using the determinative set ~~being used as~~ an address to read from.

Claim 5 (Currently Amended): Method according to ~~any of Claims Claim 1 to 4,~~ characterized in that wherein the binary sequences each ~~consist of~~ include the values +1 and -1 and, ~~apart from possible change of sign,~~ the logical combination ~~is~~ includes a multiplication with a possible change of sign.

Claim 6 (Currently Amended): Method according to Claim 5, ~~characterized in that~~ wherein the magnitude of the feedback function is 1 if the magnitudes of the arguments are each 1.

Claim 7 (Currently Amended): Method according to Claim 5 ~~or 6,~~ ~~characterized in that~~ wherein the sign of the feedback function always corresponds to the sign of the logical combination of the arguments.

Claim 8 (Currently Amended): Method according to ~~any of Claims Claim 5 to 7,~~ ~~characterized in that~~ wherein the feedback function is invariant on interchange of the arguments.

Claim 9 (Currently Amended): Method according to ~~any of Claims Claim 5 to 8,~~ ~~characterized in that~~ wherein the feedback function is antisymmetric and monotonic as a function of each argument.

Claim 10 (Currently Amended): Method according to ~~any of Claims Claim 5 to 9,~~
~~characterized in that~~ wherein the feedback function is substantially a linear combination of
the arguments within substantially each sector characterized by specific values of the signs of
the arguments.

Claim 11 (Currently Amended): Method according to Claim 10, ~~characterized in that~~
wherein the magnitude of the feedback function substantially corresponds to the mean value
of the magnitudes of the arguments.

Claim 12 (Currently Amended): Method according to ~~any of Claims Claim 6 to 11,~~
~~characterized in that~~ further comprising:

producing the feedback value is produced by multiplication of the value of the
feedback function with a factor $k < 1$, which is preferably between 0.90 and 0.99.

Claim 13 (Currently Amended): Method according to ~~any of Claims Claim 5 to 12,~~
~~characterized in that~~ wherein the determinative set ~~consists of the~~ includes binary values
which in each case have ~~the a~~ same sign as ~~the a~~ corresponding analog value $(a_{i-n}; \dots; a_{i-1})$ in
the analog shift register.

Claim 14 (Currently Amended): Method according to ~~any of Claims Claim 1 to 13,~~
~~characterized in that~~ further comprising:

deriving a basic sequence from the received signal, the external sequence ~~corresponds~~
corresponding to a plurality of copies, directly in succession with respect to time, of a the
basic sequence ~~which is derived from the received signal, the~~ and a length of which each of
the plurality of copies corresponds to the length N of the fundamental sequence.

Claim 15 (Currently Amended): Method according to Claim 14, ~~characterized in that~~
further comprising:

generating the basic sequence ~~is generated by~~ adding the values of a plurality of
sequences of length N which are derived successively from the received signal.

Claim 16 (Currently Amended): Method according to ~~any of Claims~~ Claim 1 to 15,
~~characterized in that~~ further comprising:

generating a binary output signal indicating complete synchronization ~~is generated if~~
the magnitudes of ~~the~~ values (a_i) of the internal sequence exceed a threshold value.

Claim 17 (Currently Amended): Synchronization circuit for carrying out ~~the a~~
received signal synchronization method as claimed in any of claims 1 to 16, said circuit
comprising:

an analog feedback shift register having an input for receiving an ~~configured to~~
receive an external sequence of analog values ~~which is derived from a~~ the received signal and
~~an~~ values in the analog feedback shift register (25);

a feedback circuit (26) ~~connected thereto with~~ to taps of the analog feedback shift
register according to a specific feedback pattern and intended for evaluating ~~configured to~~
evaluate a feedback function for determining and thereby determine a feedback value[[,]];
and

a superposition circuit ~~for superposing~~ configured to superpose the feedback value
with an intermediate value, ~~characterized in that it additionally comprises;~~

a memory (29) from which ~~in each case~~ a value ~~can be~~ is configured to be read out ~~according to a table with~~ using a determinative set derived from the values stored in the analog feedback shift register (25) as a memory address[[,]]; and

a logic element (23) ~~for producing~~ configured to produce the intermediate value by logical combination of the value read ~~out from the memory~~ with ~~the~~ a value present in the external sequence of analog values at the input.

Claim 18 (Currently Amended): Synchronization circuit according to Claim 17, ~~characterized in that~~ further comprising:

a gain block (27) ~~for producing~~ configured to produce the feedback value from its ~~an~~ initial value ~~follows and connected to an output of the feedback circuit (26), and~~

wherein the superposition circuit ~~is in the form of~~ includes an adder (24) ~~for adding~~ configured to add the feedback value to the intermediate value.

Claim 19 (Currently Amended): Synchronization circuit according to Claim 17 ~~or 18~~, ~~characterized in that it comprises~~ further comprising:

a discriminator (28) ~~for generating~~ configured to generate a binary output signal indicating synchronization, ~~the~~ including an input ~~of which discriminator is connected to the~~ an output of the feedback circuit (26) ~~and which discriminator preferably comprises a squaring circuit, a low-pass filter and a threshold value detector.~~

Claim 20 (Currently Amended): Receiver for receiving a signal, ~~which comprises the~~ receiver comprising at least one synchronization circuit according to ~~any of Claims~~ Claim 17 ~~to 19~~ for deriving an internal sequence from the received signal.

Claim 21 (Currently Amended): Receiver according to Claim 20, ~~characterized in that it comprises~~ further comprising at least one pair of identical synchronization circuits, one of which is connected via an inverter (20) and the other directly to a common input.

Claim 22 (Currently Amended): Receiver according to Claim 20 ~~or 21, characterized in that it comprises~~ further comprising at least one pair of identical synchronization circuits ~~which in each case are~~ connected via a sampling element (16; 17) to a common input, ~~with the receiver further comprising a delay element (18) which shifts connected to an input of at least one sampling element and configured to shift the sampled values in each case by a part of a chip length in front of at least one sampling element (17).~~

Claim 23 (Currently Amended): Receiver according to ~~any of Claims Claim 20 to 22,~~ Claim 20 to 22, ~~characterized in that it comprises~~ further comprising:

an oscillator (12) ~~for generating~~ configured to generate a first sinewave signal and a second sinewave signal phase-shifted relative ~~thereto to the first sinewave signal~~ by 90° [[,]]; and

at least one pair of identical synchronization circuits[[,]]; and
~~each with a mixer (11; 13) in front for mixing connected to an input of each of the~~
identical synchronization circuits and configured to mix the received signal with the first sinewave signal or the second sinewave signal.

Claim 24 (New): Synchronization circuit of Claim 19, wherein the discriminator further comprises a squaring circuit, a low-pass filter and a threshold value detector.